2016
BCA
[HONOURS]
(Digital Logic & Computer Organization)
Paper : BCA-103

Full Marks : 80 Time : 4 Hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer **Question No. 1** and any **four** from the rest.

1. Answer any **eight** questions: 2×8=16

   i) Convert binary number $(101101.1101)_2$ to octal.

   ii) Design NOR gate using NAND gates only.

   iii) How many flip/flops are needed to design a mod 10 counter?

   iv) Write the differences between static and dynamic RAM.

   v) What is race problem?

   vi) Find the gray code of $(101101)_2$.

   vii) Differentiate between 1's complement and 2's complement representation.

   viii) What is CCD memory?

   ix) What is the use of Don't Care Condition?

   x) Write down the truth table of S-R Flip/Flop.

   xi) What is a ripple counter?

   xii) What is addressing mode?

2. a) Express the following function in sum of min terms and a product of max terms $F(x,y,z)=(xy+z)(y+xz)$.

   b) Perform the substraction with the following binary no's using 2's complement arithmetic:

   $$(11010)_2-(10000)_2=?$$

   c) The sum of two no's written as 13 and 22 is 101. What is the base of the number system?

   d) Show that dual of EX-NOR is equal to it's complement.

   e) Find the 10's complement of $(539)_{11}$. 5+3+3+3+2=16

3. a) Simplify the following function using K-map.

   $F(A,B,C,D)=\sum(2,3,12,13,14,15)+d(0,4,9)$.

   b) Design a full substractor circuit.

c) Implement the following function using NAND gates. Assume that both normal and complements input are available

$$F = (AB + A'B')(CD' + C'D)$$

d) Write down the differences between BCD code and EX-3 code. 5+5+4+2=16

4. a) Implement a Full adder circuit with multiplexer.

b) Design a combinational circuit to generate Even parity of four bit lengths.

c) Design a binary comparator to compare two binary numbers A & B each consisting of two bits. 5+7+4=16

5. a) Explain the operation of a S-R flip/flop. What are its limitation?

b) Design a counter with the following binary sequence : 0, 4, 2, 1, 6 and repeat. Use J-K flip/flop.

c) Explain the operation of universal shift register. 4+7+5=16

6. a) Explain the Von-Neuman architecture.

b) Discuss various data transfer techniques with the help of block diagram and timing diagram.

c) Explain the DMA transfer process briefly. 4+8+4=16

7. Write short notes (any **four**) : 4×4=16

a) Strobe based and handshare based communication

b) Virtual Memory

c) Sequential Machine design

d) Microprogrammed control unit

e) Instruction Pipelining

f) PLAs

g) BUS

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